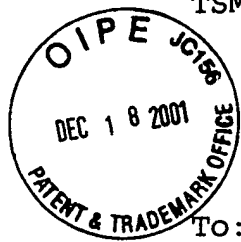


TSMC-98-850/852B



October 26, 2001

To: Commissioner of Patents and Trademarks  
Washington, D.C. 20231

Fr: George O. Saile, Reg. No. 19,572  
20 McIntosh Drive  
Poughkeepsie, N.Y. 12603

Subject:

Serial No. 09/932,680 08/20/01

C.J. Lin, H.D. Su, Jong Chen,  
W.T. Chu

TILT-ANGLE ION IMPLANT TO IMPROVE  
JUNCTION BREAKDOWN IN FLASH MEMORY  
APPLICATION

Grp. Art Unit: 2813

#### INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation  
In An Application.

The following Patents and/or Publications are submitted to  
comply with the duty of disclosure under CFR 1.97-1.99 and  
37 CFR 1.56. Copies of each document is included herewith.

U.S. Patent 5,565,369 to Ko, "Method of Making Retarded  
DDD (Double Diffused Drain) Device Structure", describes a  
method of forming a retarded double diffused drain structure,  
and the resultant retarded double diffused drain structure, for  
a field effect transistor.

2813

#3 / DS  
4-3-02  
retaken

U.S. Patent 5,793,090 to Gardner et al., "Integrated Circuit Having Multiple LDD and/or Source/Drain Implant Steps to Enhance Circuit Performance", describes an integrated circuit having multiple LDD and/or source/drain implant steps to enhance circuit performance.

U.S. Patent 5,851,869 to Urayama, "Manufacture of Semiconductor Device Having Low Contact Resistance", discloses the use of a DDD structure in the manufacture of a semiconductor device having low contact resistance.

U.S. Patent 5,498,554 to Mei, "Method of Making Extended Drain Resurf Lateral DMOS Devices", discloses a method of making an integrated circuit containing low voltage PMOS and/or NMOS devices as well as high voltage PMOS and/or NMOS devices.

U.S. Patent 5,770,502 to Lee, "Method of Forming a Junction in a Flash EEPROM Cell by Tilt Angle Implanting", discloses a method of forming a modified DDD junction structure which is formed on stack gate structure side on which a floating gate and a control gate are laminated and a non-DDD structure is formed on split gate side, by forming a first impurity region through a tilt-angle implanting of impurity ions at a high level of energy and the forming a second impurity region through a tilt-angle implanting of impurity ions at a lower level of energy using a spacer.

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U.S. Patent 5,750,435 to Pan, "Method for Minimizing the Hot Carrier Effect in N-MOSFET Devices", teaches a method for minimizing the hot carrier effect in N-MOSFET devices by implanting into the gate oxide regions beneath the gate electrode edges a dose of a hardening ion.

Sincerely,

A handwritten signature in black ink, appearing to read 'SBA', is written over the printed name.

Stephen B. Ackerman,  
Reg. No. 37761